A Novel Deep Trench Isolation Featuring Airgaps for a High-Speed 0.13µm SiGe:C BiCMOS Technology

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ABSTRACT

A novel scheme for deep trench isolation is presented, which uses an airgap as insulator. When incorporated in our 0.13µm SiGe:C BiCMOS technology, the peripheral substrate parasitics decrease with an order of magnitude to a record value of 0.02fF/µm, which significantly improves the device RF performance.

INTRODUCTION

Over the past few years, SiGe:C HBTs have made a tremendous improvement in RF performance. Reduction of device parasitics is key for obtaining even higher speed. Smart device architectures have been conceived to reduce device parasitics, including raising the extrinsic base regions [1], cutting away unnecessary active device regions [2] or using double poly architectures with selectively grown base epitaxial layers [3]. Ever since deep trench isolation (DTI) was invented, a strong reduction of the collector-substrate capacitance (C_{cs}) was obtained through a reduction of the collector area and the perimeter specific collector-substrate capacitance density ($C_{cs,p}$). The latter is usually obtained by partially filling the deep trench with oxide, which has a low κ-value, and the remainder with polysilicon, which acts as a stress-relief buffer. In this work however, we use an airgap to isolate devices. The integration scheme is fully compatible with standard STI processing and does not require novel materials or complex processing steps. Integrating the airgap DTI module in a high-speed SiGe:C BiCMOS technology, we will show the isolation properties and the impact on device performance.

DEEP TRENCH ISOLATION PROCESSING

The fabrication of the deep trench isolation module is illustrated in Figure 1. On top of the STI oxide-nitride stack, a thick oxide layer is deposited, which is used as a hardmask to etch the deep trench (a). The trench is 1µm wide and 6µm deep. The trench is filled with oxide and polysilicon. Then the wafer is planarized using CMP, stopping on the oxide layer. After creation of a recess in the polysilicon plug (b), D-shape oxide spacers are created inside the deep trench. Subsequently, the underlying polysilicon is completely removed by dry etch using an isotropic SF_6 chemistry (c). The purpose of the spacers is to narrow down the trench opening, which allows an easy trench closing by depositing oxide. Then the wafer is polished again, stopping on the nitride layer (d). Figure 2 shows a cross-section SEM picture after this second planarization step. After this step, the original state of the wafer is restored and the shallow trench isolation (STI) module can be processed. One of the key features of this DTI module is that the STI module can be processed without any modification of the processing steps. Figure 3 shows a TEM picture of the complete HBT at the end of processing.

ISOLATION PROPERTIES

The collector-substrate isolation is illustrated in Figure 4, where the leakage current is plotted versus bias. The leakage level is low and comparable with the case where no deep trenches are present. This means that the presence of the deep trench did not introduce additional leakage. The collector-collector isolation is depicted in Figure 5. In this kind of structures where two n-type regions in a p-type substrate are separated by a deep trench, a parasitic conduction channel around the deep trench is present [4]. Due to the absence of a polysilicon plug in the deep trench, there is no gate that can turn on this channel. With a collector-substrate and collector-collector breakdown voltage exceeding 100V, the airgap DTI is superior to classical DTI schemes using an oxide/polysilicon filling and is also suitable for high voltage applications. The collector-substrate capacitance associated with the airgap isolation is strongly reduced due to a reduction in $C_{cs,p}$. Figure 6 compares $C_{cs,p}$ for different isolation schemes. At reverse bias, a value of 0.02fF/µm is obtained for the airgap DTI, which is an order of magnitude lower than for classical DTI schemes.

DEVICE RESULTS

To demonstrate the impact of the airgap DTI on device performance, the module is incorporated in our high-speed 0.13µm SiGe:C BiCMOS technology. The architecture for this technology is based on a low-complexity quasi-self-aligned integration scheme, which was recently scaled down vertically and laterally towards high-speed operation [5]. A typical Gummel plot is shown in Figure 7 and shows only a slight impact of the airgap isolation on DC device characteristics. Despite the lateral confinement of the heat-flux by the airgap, the devices are thermally very stable. The thermal resistance R_{TH} for a 0.13µmx2µm device is about 12.6kK/W, which is only slightly higher than the value for classical DTI schemes (Figure 8). Figure 9 shows the relative increase of C_{cs} with decreasing device length in comparison with the base-emitter and base-collector capacitances C_{be} and C_{bc}. It is clear that using the airgap DTI allows controlling the substrate parasitics as device dimensions are scaled down. Figure 10 shows the cut-off frequency f_T and the maximum oscillation frequency f_{max} versus collector current. Peak f_T/f_{max} values exceeding 200GHz are obtained. An excellent figure-of-merit to study the impact of the airgap DTI is the recently introduced available bandwidth f_A [6], which gives a more realistic idea of the device RF performance in real circuit blocks like for instance emitter-coupled pairs. In comparison with classical DTI schemes, the airgap isolation improves the peak f_A value with 17% (Figure 10). At low power, the device RF performance is heavily impacted by parasitic capacitances. The airgap isolation boosts up the low-power f_A value with 75%.

CONCLUSIONS

We have demonstrated the integration of a novel airgap DTI module into a BiCMOS process, which is fully compatible with standard STI processing. Without affecting the thermal stability of the devices, the airgap strongly reduces the substrate parasitics, allowing significant improvement in device RF performance.

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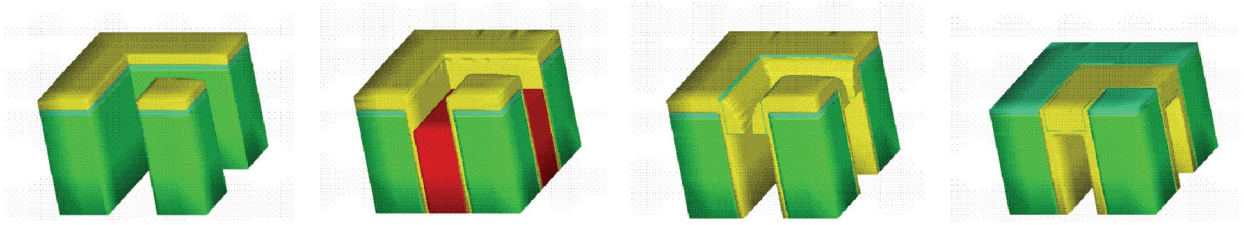

Fig.1: Overview of the airgap processing: (a) after trench etch and liner oxidation, (b) after trench fill and recess formation in the polysilicon plug, (c) after spacer formation and trench clearing and (d) after trench closing and planarization.

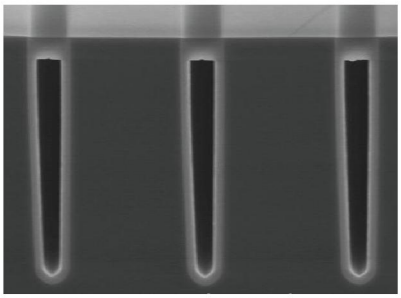

Fig.2: Tilted cross-section SEM picture at the end of the airgap DTI module.

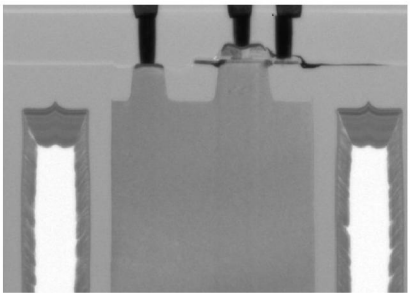

Fig.3: TEM picture at the end of processing, the airgap deep trench isolates the HBT.

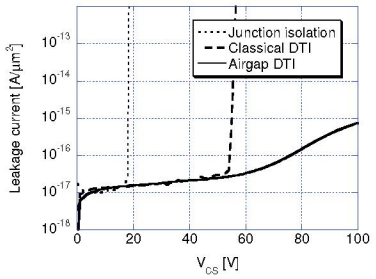

Fig.4: Collector-substrate leakage for different isolation schemes.

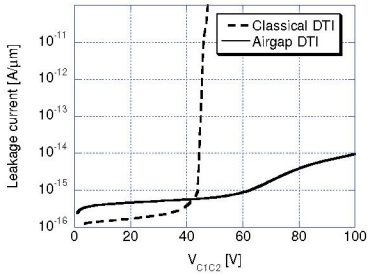

Fig.5: Collector-collector leakage for different types of DTI. Measured between two collectors separated by a deep trench.

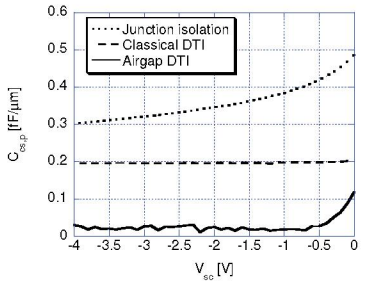

Fig.6: Perimeter specific collector-substrate capacitance density $C_{cs,p}$ for different isolation schemes.

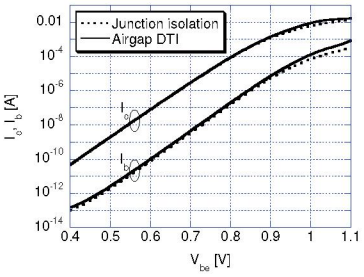

Fig.7: Typical gummel plot for a device with A_E=0.13µmx2µm. Measured at V_{cb}=0V.

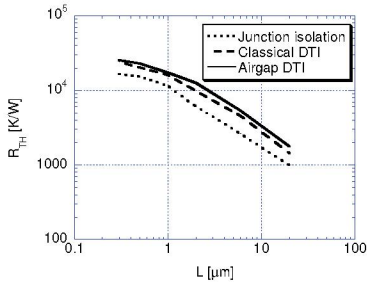

Fig.8: Thermal resistance for devices with a minimum emitter width of 0.13µm and various lengths.

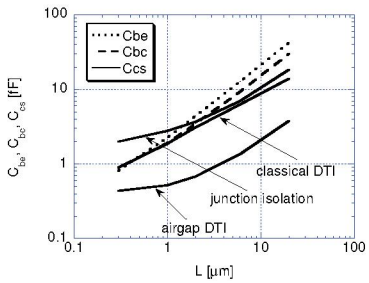

Fig.9: C_{be} and C_{bc} at zero bias and C_{cs} at 1V reverse bias for devices with a minimum emitter width of 0.13µm and various lengths.

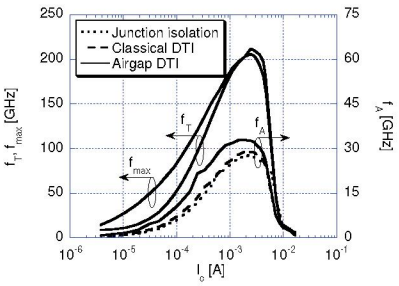

Fig.10: F_T, f_{max} and f_A vs. I_c for a device with A_E=0.13µmx2µm. Measured at V_{cb}=0.5V. F_A is the available bandwidth for a DC gain of 10.