Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal FinFETs Having Flexible Threshold Voltage and Good Subthreshold Slope

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***Abstract*—Flexibly controllable threshold-voltage ($V_{\rm th}$) asymmetric gate-oxide thickness ($T_{\rm ox}$) four-terminal (4T) FinFETs with HfO_2 [equivalent oxide thickness (EOT) = 1.4 nm] for the drive gate and HfO_2 + thick SiO_2 (EOT = 6.4–9.4 nm) for the $V_{\rm th}$-control gate have been successfully fabricated by utilizing ion-bombardment-enhanced etching process. Owing to the slightly thick $V_{\rm th}$-control gate oxide, the subthreshold slope (S) is significantly improved as compared to the symmetrically thin $T_{\rm ox}$ 4T-FinFETs. As a result, the asymmetric $T_{\rm ox}$ 4T-FinFETs gain higher $I_{\rm on}$ than that for the symmetrically thin $T_{\rm ox}$ 4T-FinFETs under the same $I_{\rm off}$ conditions.**

***Index Terms*—Asymmetric gate-oxide thickness, FinFET, four-terminal (4T) FinFET, ion-bombardment-enhanced etching (IBEE), subthreshold slope, threshold-voltage control.**

I. Introduction

POSTFABRICATION threshold-voltage ($V_{\rm th}$) tuning is the essential technology to overcome catastrophic increases in static-power consumption especially in ubiquitous electronics very large scale integrated circuits. Among many $V_{\rm th}$-controllable devices, an independent double-gate (DG)-FinFET (named "4-terminal-FinFET" because of its four terminals: S; D; G1; and G2) [1]–[3] is expected to be one of the best choices because of its following advantages. The $V_{\rm th}$ in 4T-FinFETs can be controlled not only backwards but also forwards. This enables the $I_{\rm on}/I_{\rm off}$ performance to flexibly range from an active state to a standby state. Since each four-terminal (4T)-FinFET has an independent $V_{\rm th}$-control gate, the $V_{\rm th}$ for each transistor can be controlled individually. Furthermore, a much faster $V_{\rm th}$ control can be expected for the 4T-FinFET because of the very small G2, i.e., $V_{\rm th}$-control gate. Previously reported 4T-FinFETs [1]–[3] had symmetrically thin gate oxides on both channels, unfortunately resulting in large subthreshold slope (S) due to the negative effect of the high second gate (G2) controllability [4]. To attain a good S even after DG separation, the asymmetric gate-oxide thickness ($T_{\rm ox}$) (thin drive-gate $T_{\rm ox}$ and slightly thick $V_{\rm th}$ control gate $T_{\rm ox}$) has been suggested [5]. However, no one could realize this structure, because both gate stacks were simultaneously formed in a conventional FinFET fabrication process.

This letter demonstrates, for the first time, asymmetric $T_{\rm ox}$ 4T-FinFETs with HfO_2 (EOT = 1.4 nm) for one side and HfO_2 + thick SiO_2 (EOT = 6.4–9.4 nm) for the other side fabricated using a novel ion-bombardment-enhanced etching (IBEE) process [6]. The superiority of the asymmetric $T_{\rm ox}$ 4T-FinFET over the symmetrically thin $T_{\rm ox}$ 4T-FinFETs is experimentally demonstrated.

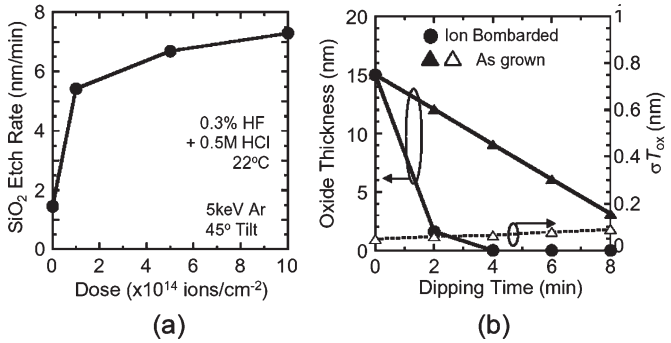

Fig. 1. (a) Dependence of SiO_2 etch rate in pH-controlled dHF/HCl mixture on Ar-ion-implantation dose. (b) Changes in ion-bombarded-SiO_2 (circles) and as-grown SiO_2 thicknesses (triangles) and standard deviation σ of as-grown SiO_2 thickness (open triangles) during the etching. The SiO_2 etch rate is significantly enhanced by Ar-ion implantation. The pH-controlled dHF/HCl mixture ensures unchanging σ of as-grown SiO_2 during the etching.

II. Device Fabrication

The asymmetric $T_{\rm ox}$ gate stack was realized using Ar-IBEE of SiO_2 [6]. As shown in Fig. 1(a), the etch rate of SiO_2 in a 0.3% diluted HF/HCl mixture [7] is significantly enhanced by Ar-ion bombardment. The etching enhancement of SiO_2 in HF originates in the Si–O bond breaking due to the ion implantation [6]. The fabrication process flow for the asymmetric $T_{\rm ox}$ 4T-FinFETs is shown in Fig. 2. Fin channels were fabricated

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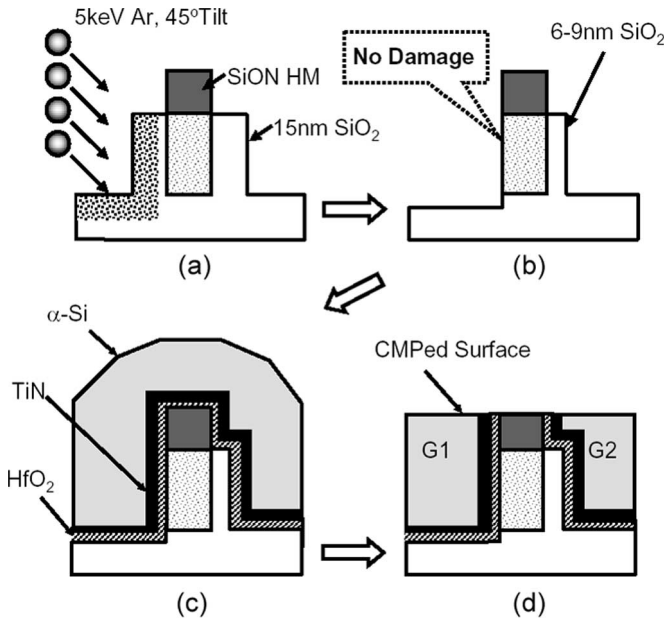

Fig. 2. Schematic fabrication process flow for asymmetric $T_{\rm ox}$ ($T_{\rm ox1} < T_{\rm ox2}$) 4T-FinFETs. (a) Fin channel Ox. and tilted I/I. (b) IBEE in dHF. (c) Gate stack and SD formation. (d) DG separation by CMP.

on 8-in (100)-SOI wafers with 65-nm Si films on top of 145-nm buried oxide. The 15-nm-thick SiO_2 growth on both side channels was followed by 5-keV Ar tilted implant with 5×10^{14} cm^{-2} on one side. The SiO_2 thickness, ion energy, and dose were adjusted so that Ar ions did not damage the Si channel. Then, the samples were dipped in a pH-controlled diluted HF/HCl mixture, where ion-bombarded SiO_2 was completely removed from one side after 4 min while thick SiO_2 still remained on the other side, as shown in Fig. 1(b). Note that the pH-controlled diluted HF/HCl mixture ensures unchanging uniformity of as-grown SiO_2 thickness, i.e., $V_{\rm th}$-control gate-oxide thickness, during etching. Then, Atomic Layer Deposition HfO_2 (EOT = 1.4 nm) was deposited. As a result, the first gate oxide ($T_{\rm ox1}$) became 1.4 nm. The second gate-oxide thickness ($T_{\rm ox2}$) was varied from 6.4 to 9.4 nm by adjusting the etching time of SiO_2. After that, metal–organic chemical-vapor-deposited TiN (5 nm) and amorphous Si (200 nm) were deposited and etched back to 60 nm to reduce topography [8]. After gate patterning, the source and the drain were formed with conventional ion implantation followed by spacers and Ni salicidation. As the last step, Chemical Mechanical Polishing (CMP) was employed to separate the gates, stopping in the 40-nm SiON layer protecting the fin. No channel doping and no halo implantation were employed. Both PMOS and NMOS were fabricated. Here, we focus on PMOS data. Note that similar effect was confirmed for NMOS. The gate length (L_g) is 75 nm. The fin height ($H_{\rm Fin}$) and thickness ($T_{\rm Fin}$) are 65 and 30 nm, respectively.

III. Results and Discussion

Fig. 3 shows the cross-sectional scanning transmission electron microscope (STEM) image of the fabricated asymmetric $T_{\rm ox}$ 4T-FinFETs. It can be confirmed that the double gates

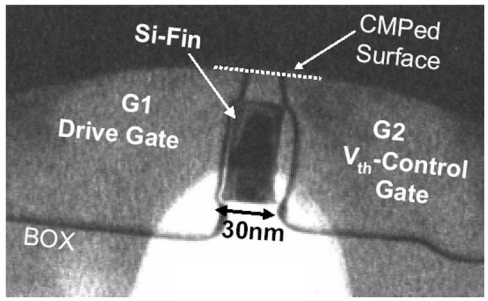

Fig. 3. Cross-sectional STEM image of the fabricated asymmetric $T_{\rm ox}$ 4T-FinFET. The asymmetric gate oxides ($T_{\rm ox1} < T_{\rm ox2}$) are successfully incorporated into the 4T-FinFET.

are completely separated and asymmetric $T_{\rm ox}$ ($T_{\rm ox1} < T_{\rm ox2}$) is successfully formed. Here, we define the left gate (G1) as a drive gate and the right gate (G2) as a $V_{\rm th}$-control gate. Fig. 4 shows the measured I_d–V_{g1} characteristics and the $V_{\rm th}$ (V_g at $I_d = W/L \times 10^{-7}$ A/μm) and S as a function of V_{g2} for the fabricated 4T-FinFETs. Note that I_d was normalized by $H_{\rm Fin}$ for the 4T mode while $2^* H_{\rm Fin}$ for the 3T mode because C_g for the 4T-FinFETs is a half of C_g for the 3T-FinFET. Both the symmetric and the asymmetric $T_{\rm ox}$ 4T-FinFETs clearly exhibit flexible $V_{\rm th(G1)}$ ($V_{\rm th}$ in the 4T mode) controllability by V_{g2} as shown in Fig. 4(a) and (b). Relatively high $V_{\rm thDG}$ ($V_{\rm th}$ in the 3T mode) originates in the workfunction of the TiN metal gate. For both cases, $I_{\rm off}$ can be controlled from a stand-by ($I_{\rm off} = 10^{-11}$ A/μm) to an active state ($I_{\rm off} = 10^{-7}$ A/μm). For the symmetric $T_{\rm ox}$ case, $I_{\rm off}$ increases with increasing V_{g2}, as shown in Fig. 4(a). This is due to the leakage current through the G2 insulator as can be understood from I_{g2} curves in Fig. 4(a). In contrast, for the asymmetric $T_{\rm ox}$ case, $I_{\rm off}$ is successfully suppressed owing to the slightly thick $T_{\rm ox2}$. As shown in Fig. 4(c), the $V_{\rm th(G1)}$ shift rate ($\gamma = dV_{\rm th(G1)}/dV_{g2}$) becomes lower and, thus, S is improved with increasing $T_{\rm ox2}$ in any V_{g2} condition. Especially, S is dramatically decreased in the G2 inversion condition (V_{g2} being larger than $V_{\rm thDG}$, that is, $V_{\rm th(G1)}$ being less than $V_{\rm thDG}$). This is because S is determined by the G2-side surface potential in this condition [9]. Analytically, S in the G2 depletion condition is given by $60\{1 + 3T_{\rm ox1}/(3T_{\rm ox2} + T_{\rm Fin})\}$ [mV/dec]. On the other hand, it turns to $60\{1 + (3T_{\rm ox1} + T_{\rm Fin})/3T_{\rm ox2}\}$ [mV/dec] in the G2 inversion condition [9]. Thus, S is greatly improved by slightly increasing $T_{\rm ox2}$ in the G2 inversion condition. Fig. 5 shows I_d–V_d curves for the symmetric and asymmetric $T_{\rm ox}$ 4T-FinFETs under the same $I_{\rm off}$ condition. Obviously, the asymmetric $T_{\rm ox}$ 4T-FinFET gains higher $I_{\rm on}$ than that for the symmetric $T_{\rm ox}$ one because of the higher gate over drive ($V_{\rm dd} - V_{\rm th(G1)}$) due to the improved S. Also, it should be noted that 4T-FinFETs show greatly higher $I_{\rm on}$ as compared to the 3T-FinFET at an active state. As for the drive gate oxide (thin $T_{\rm ox1}$), the ion-bombarded SiO_2 was completely removed and then HfO_2 layer was deposited. As for the $V_{\rm th}$-control oxide (thick $T_{\rm ox2}$), according to [7], the etched-back SiO_2 maintains the same property as virgin SiO_2. As for Si fin channel, Ar dose and energy were adjusted so that Ar ions could not pass through the SiO_2 and could not penetrate into the Si channel. We also confirmed that the IBEE-processed asymmetric $T_{\rm ox}$ 4T-FinFETs with a long L_g showed the same

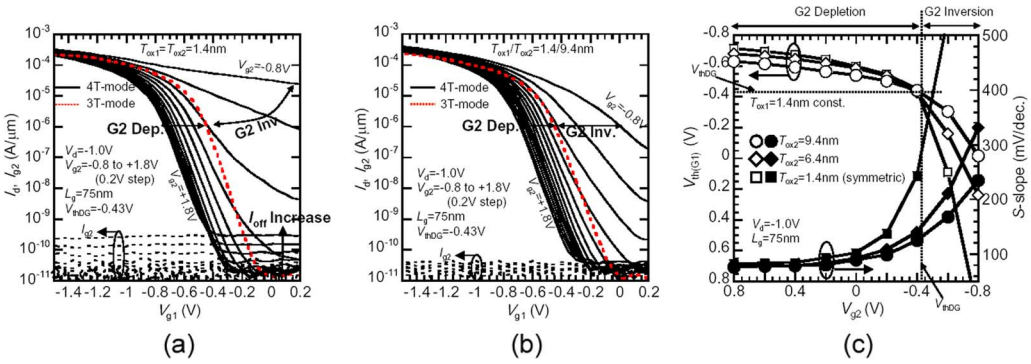

Fig. 4. I_d–V_{g1} characteristics for (a) symmetric $T_{\rm ox}$[$T_{\rm ox1} = T_{\rm ox2} = 1.4$ nm (EOT)], (b) asymmetric $T_{\rm ox}$ [$T_{\rm ox1} = 1.4$ nm (EOT), $T_{\rm ox2} = 9.4$ nm (EOT)] PMOS 4T-FinFETs, and (c) $V_{\rm th}$ and S as a function of V_{g2}. In the 4T mode, G1 was used as the drive gate while G2 as the $V_{\rm th}$-control gate. In the 3T mode, both G1 and G2 were driven simultaneously. As $T_{\rm ox2}$ increases, $\gamma(= dV_{\rm th(G1)}/dV_{g2})$ becomes lower, and the S is dramatically improved especially in the G2 inversion condition ($V_{\rm th}$(G1) being less than $V_{\rm thDG}$, where $V_{\rm thDG}$ is $V_{\rm th}$ in the 3T mode).

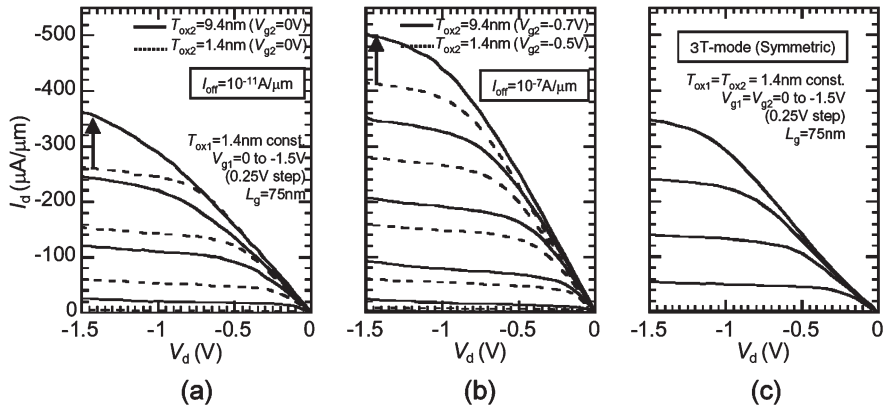

Fig. 5. I_d–V_d characteristics for asymmetric and symmetric $T_{\rm ox}$ 4T-FinFETs under the same $I_{\rm off}$ condition. (a) $I_{\rm off} = 10^{-11}$ A/μm. (b) $I_{\rm off} = 10^{-7}$ A/μm. (c) I_d–V_d characteristics for symmetric-$T_{\rm ox}$ 3T-FinFET. Owing to the improved S, higher $I_{\rm on}$ can be obtained for the asymmetric $T_{\rm ox}$ 4T-FinFET. At an active state, 4T-FinFETs show greatly higher $I_{\rm on}$ as compared to the 3T-FinFET.

linear-mode transconductance (g_m) as the non-IBEE-processed symmetric-$T_{\rm ox}$ ones. This proves that implanted Ar ions did not damage the Si channel at all during IBEE process. From these results, we now consider that the proposed fabrication process for the asymmetric $T_{\rm ox}$ 4T-FinFET does not cause any issues such as lowering of the dielectric reliability.

IV. Conclusion

For the first time, flexibly $V_{\rm th}$-controllable asymmetric $T_{\rm ox}$ 4T (separated DG)-FinFETs with HfO_2 (EOT = 1.4 nm) for the drive gate and HfO_2 + thick SiO_2 (EOT = 6.4–9.4 nm) for the $V_{\rm th}$-control gate have been successfully demonstrated. Owing to the slightly thick $V_{\rm th}$-control gate oxide, the S is significantly improved as compared with the symmetrically thin $T_{\rm ox}$ 4T-FinFETs. As a result, the asymmetric $T_{\rm ox}$ 4T-FinFETs gives higher $I_{\rm on}$ than that for the symmetrically thin $T_{\rm ox}$ 4T-FinFETs.

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